Patent
Attorney's Docket No. 014823-116

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Shawn Smith, et al.	)	Group Art Unit: 2784
	)	
Application No.: 09/192,164	)	Examiner: Greene, J.
	)	
Filed: November 13, 1998	)	
	)	
For: IC TEST SOFTWARE SYSTEM FOR MAPPING LOGICAL FUNCTIONAL TEST DATA OF LOGIC INTEGRATED CIRCUITS TO PHYSICAL REPRESENTATION	)	

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to Commissioner of Patents, Washington, D.C. [illegible] June 5, 2000
MARIA REGINA CATILO
6-5-2000

RESPONSE UNDER 37 CFR §1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Responsive to the Office Action of February 3, 2000, please amend this application as follows:

IN THE CLAIMS:

1. (Amended) A method of automated defect localization in the testing of semiconductor integrated circuits, comprising the steps of:

testing the integrated circuits to obtain generalized failure data;

inputting the generalized failure data and circuit models describing logical operations of the integrated circuits to a circuit analysis tool;

obtaining from the circuit analysis first localized probable defect data;

performing in-line inspection of the integrated circuits to obtain second localized probable defect data; and

correlating the first and second localized probable defect data.